REMARKS

In this Response, claims 1-3 and 5 are amended, and new claim 7 is presented. The applicants respectfully submit that the amendments and the added claim are fully supported by the originally filed application and that no new matter has been added. Claims 1-7 are presented for examination.

Rejections Under 35 U.S.C. § 103

Claims 1-6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Curry et al. (US 6,112,275) in combination with Smith et al. (US 6,762,733). The applicants respectfully traverse the rejection for at least the following reasons.

Claim 1 has been amended and is now is directed towards a programmable interface that includes, among other features:

a microcontroller configured to bidirectionally communicate with the register file and the run control register;

a Code Store SRAM configured to bidirectionally communicate with the microcontroller;

... the run control register are configured to bidirectionally communicate with a system processor.

Thus, the claim recites a *run control register* to bidirectionally communicate with a *microcontroller* **and** *a system processor.* For example, the applicants' Fig. 1 illustrates a run control register 16 communicating with main system CPU 30 and microcontroller 12. Such a configuration has certain advantages, some of which are disclosed in the applicants' specification, e.g., paragraph 14, lines 4-5; and paragraph 02, lines 7-8.

The Examiner appears to allege that Curry discloses microcontrollers 2414 and 2404 in Fig. 24 and the Master microprocessor of Fig. 37A, where the Master microprocessor of Fig. 37A bidirectionally communicates with a 1-3 wire convertor, which includes a ROM and control 2108 (Curry, col. 64, lines 53-58). The Examiner appears to equate the Master microprocessor and the ROM and control 2108 (included in the 1-3 wire convertor) with the recited *microcontroller* and the *Code Store SRAM,* respectively.

The Examiner acknowledges that Curry does not disclose a *run control register;* and also does not disclose *the run control register configured to bidirectionally communicate with a system processor,* but alleges that Smith does disclose these elements. Specifically, the Examiner appears to equate Smith's registers 160, 162, and 164 (coupled to the NVRAM controller 170 or EEPROM controller 172, Fig. 7) to the recited *run control* register. It is unclear to the applicants where Smith discloses that the registers 160, 162, and 164 correspond to a *run control register* that communicates with a *system processor.* A person of ordinary skill in the art would appreciate the difference between a memory controller (e.g., Smith's NVRAM controller 170 or EEPROM controller 172) and the recited *system processor.* Although Smith's registers 160, 162, and 164 communicate with a memory controller (NVRAM controller 170 or EEPROM controller 172), Smith does not disclose registers 160, 162, and 164 bidirectionally communicating with a system processor, as required by claim 1.

Additionally, the Examiner alleges that it would be obvious to combine Smith's teaching (registers 160, 162, and 164 communicating with the memory controller) with Curry's system (Master microprocessor of Fig. 37A) to achieve the claimed invention, the motivation for combining being permitting hotel guests to actively participate in video game play or to use other data processing/communication service. The applicants fail to understand how such motivation may be used to combine Smith's teaching with that of Curry to arrive at the specific claimed features. Permitting hotel guests to actively participate in video game play or to use other data processing/communication service does not specifically require configuring Smith's registers 160, 162, and 164 (the alleged *run control register*) to communicate with Curry's Master microprocessor of Fig. 37A (the alleged *microcontroller).* It is not simply a matter of the presence of all the claimed elements in the art, but rather an explanation of how one of ordinary skill in the art would be motivated to make the specific combination of reference elements to achieve the claimed configuration. It appears that the Examiner's attempt to combine the elements of the references amounts to improper hindsight reconstruction using applicants' disclosure as a roadmap to arrive at the claimed features. And hence, neither Curry nor Smith, either alone or in combination, disclose or even suggest a *run*

control register that bidirectionally communicates with a *microcontroller* and a *system processor.*

Further, claim 1 has been amended to clarify that *the system processor is … configured to signal the microcontroller, via the run control register, to begin execution of one or more instructions included in the executable code.* As previously discussed, neither Smith nor Curry, either alone or in combination, disclose or even suggest a *run control register* coupled to a *system processor* and a *microcontroller.* For at least the same reason, neither of the two cited references, alone or in combination, discloses or suggests that the *system processor* signals the *microcontroller* via the *run control register* to begin execution of one or more instructions, as recited in claim 1.

Moreover, claim 1 recites

a Code Store SRAM configured to bidirectionally communicate with the microcontroller;

executable code, loaded onto the Code Store SRAM;

… the system processor is configured to load the executable code onto the Code Store SRAM …

As previously discussed, the Examiner appears to equate Curry's Master microprocessor and ROM and control 2108 (included in the 1-3 wire convertor) of Fig. 37A with the recited *microcontroller* and the *Code Store SRAM,* respectively. Additionally, the Examiner cites the following to allege that Curry discloses the recited loading of the executable code in the SRAM:

"Counter 2810 can be read over the 1-wire bus by a host in a manner similar to reading the RAM of module 2100: the host resets module 2800 (counter 2810 does not reset except by a command in the command register), and then loads the Read Counter command into the command register and then reads the contents of counter 2810." (Col. 57, lines 26-32).

It appears that the Examiner is now equating Curry's loading of the read counter command in the command register to the recited *executable code, loaded onto the Code Store SRAM.* That is, now the Examiner is equating curry's command register with the recited *Code Store SRAM.* On the other hand, the Examiner had earlier equated Curry's ROM and control 2108 with the recited *Code Store SRAM.* Put differently, the Examiner equates two different components (ROM and control 2108, and command register) of Curry with the recited *Code Store SRAM* while discussing two

different features of the *Code Store SRAM*. And hence, the Examiner has failed to identify a *Code Store SRAM* in Curry that *communicates with the microcontroller* **and** is loaded with *executable code*.

For at least these reasons, the applicants respectfully submit that neither Curry nor Smith, alone or in combination, discloses or even suggests claim 1, and accordingly, claim 1 is in condition for allowance, along with associated dependent claims 2-6.

New Claim

New claim 7 has been added, which is directed towards a programmable interface that includes, among other features, a *system processor* that is *configured to bidirectionally communicate with the register file*. Note that claim 1, from which new claim 7 depends, recites *a microcontroller configured to bidirectionally communicate with the register file*... Thus, claim 7 recites a register file that bidirectionally communicates with a system processor and a microcontroller.

While rejecting claim 1, the Examiner alleges that Curry's protocol registers 920 of Figs. 9A and 9B disclose the recited *register file*. Curry's protocol registers 920, however, do not communicate with a system processor (the protocol registers 920 do not even communicate with a microcontroller). Further, in the office action, the Examiner has identified several other registers (e.g., command register of module 2400 communicating with the microcontroller 2404 of Fig. 24). Curry, however, does not disclose a register file that bidirectionally communicates with a system processor and a microcontroller.

Conclusion

For at least these reasons, a Notice of Allowance is respectfully requested. If the Examiner has any questions concerning the present paper, the Examiner is kindly requested to contact the undersigned at (503) 796-2084. If any fees are due in connection with filing this paper, the Commissioner is authorized to charge Deposit Account No. 500393.

Respectfully submitted,

SCHWABE, WILLIAMSON & WYATT, P.C.

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/Kevin T. LeMond/
Kevin T. LeMond
Reg. No. 35,933

Pacwest Center, Suite 1900
1211 SW Fifth Avenue
Portland, Oregon 97204
Telephone: 503-222-9981